



Attorney Docket No.: CYPR-
CD01208M

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Craig Nemecek

Group Art Unit: 2123

Filed: November 19, 2001

Examiner: Sharon, A.

Application No.: 09/989,777

Title: SLEEP AND STALL IN AN IN-CIRCUIT EMULATION SYSTEM

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	2002/0052729	05-02-2002	Kyung et al.			
	B	2002/0156998	10-24-2002	Casselman			
	C	2003/0056071	03-20-2003	Triece et al.			
	D	2003/0149961	08-07-2003	Kawai et al.			
	E	4,176,258	11-27-1979	Jackson			
	F	4,757,534	07-12-1988	Matyas et al.			
	G	5,357,626	10-18-1994	Johnson et al.			
	H	5,691,898	11-25-1997	Rosenberg et al.			
	I	5,802,290	09-01-1998	Casselman			
	J	6,016,563	01-18-2000	Fleisher			
	K	6,034,538	03-07-2000	Abramovici			
	L	6,460,172	10-01-2002	Insenser Farre et al.			
	M	6,816,544	11-09-2004	Bailey et al.			
	N	6,967,960	11-22-2005	Bross et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	O							
	P							
	Q							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	Sreeram Duvvuru and Siamak Arya, "Evaluation of a Branch Target Address Cache", 1995, IEEE, pages 173-180
	S	Andrew S. Tanenbaum with contributions from James R. Goodman, "Structured Computer Organization", 1999, Prentice Hall, Fourth Edition, pages 264-288, 359-362
	T	Wikipedia- Main Page, retrieved on March 8, 2006 from http://en.wikipedia.org/wiki/Main_Page and http://en.wikipedia.org/wiki/Wikipedia:Introduction
	U	Wikipedia- Processor register, retrieved on March 7, 2006 from http://en.wikipedia.org/wiki/Processor_register
	V	Jonathan B. Rosenberg, <u>How Debuggers Work</u> , John Wiley & Sons, Inc., 1996, pages i-256
Examiner		Date Considered